The road to a multi-billion Euro market in Integrated Photonics

JePPIX ROADMAP 2015
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Executive Summary

The generic foundry approach is initiating a revolution in micro and nanophotonics, just as it did in microelectronics more than thirty years ago. There is no doubt that generic integration causes a dramatic reduction in the entry costs when applying Photonic ICs in novel or improved products and brings them within reach for many SMEs and larger companies.

So far, most applications have been in the field of telecommunications and data communications, but presently they are becoming much broader; examples are fibre sensor readout units, gas sensors, medical diagnostics, metrology, THz and antenna systems (Section 2).

The business case for many companies targeting Photonic ICs (PICs) in novel or improved products is a strong one. We also see a rapidly growing market for PIC designers. For foundries manufacturing generic PICs there will be an increasingly attractive business case as the market volume of PICs grows. However, in the start-up phase, which may last a few years, foundry operation will desirably be combined with other chip based products and services (Section 3).

In the coming years we foresee a further increase in the performance and the maturity of the four JePPIX foundry platforms (provided by Oclaro, Fraunhofer HHI, SMART Photonics and LioniX), to a level where the technology will be extremely competitive with application-specific processes. The development of process capabilities and performance will be accompanied by the development of sophisticated, fab-calibrated, Process Design Kits which will provide the users with models and tools for accurate and efficient design of Photonic ICs. Standardized packages are also being developed within the JePPIX community. Access to a high performance package available at a reasonable cost is equally important for rapid prototyping and product development (Sections 4, 5 and 6).

Through the application of the generic foundry model the entry costs for development of a PIC prototype are dramatically reduced, down to a level that is affordable for many SMEs and universities. It is shown that for developing prototypes, and also for low to medium volume manufacturing, InP PICs may be more cost effective than silicon photonics PICs, contrary to the widespread belief that InP technology is inherently much more expensive (Section 7).

The first generic PIC based products will become commercially available this year (2015). Based on the rapid development of industry participation in MPW runs we expect that the PIC enabled market will develop into a billion euro market before 2020 (Section 8).

The anticipated growth of the market will demand a rapidly growing number of PIC designs and hence designers. A more than tenfold increase of the present design capacity will be required within the next few years. Training and educational activities must, therefore, have high priority (Section 9).

Very significant investments in photonic foundries have been announced recently in the US. For Europe to retain its competitive edge, continued public and private investment is important. Funding should focus on raising awareness of the opportunities that Photonic ICs offer for novel or improved products for a wide range of applications, increasing training and education capacity and creating proper conditions for enabling PIC foundries to provide the required manufacturing services (Section 10).

JePPIX is playing a central role in the eco-system for foundry-based PIC development and manufacturing (Section 11). Because of the large overlap in skills and tools for designing InP and TriPleX chips, and the increasing synergy between the two technologies in the field of packaging and hybrid platform technology, JePPIX is taking the role of brokering organisation for both InP and TriPleX technology.
1. Introduction

Photonics is a rapidly growing technology: LED lighting, solar cells, displays, optical communication, optical sensors and imaging are increasingly penetrating our world. 2015 has been named the international year of light. Photonics has been recognized by the European Union as a Key Enabling Technology (KET), a technology that enables a market that is many times larger than the market of the technology itself. Micro and nano-electronic integration technology is an example of a KET which has a huge impact on our modern society; it is applied almost everywhere. Integrated photonics has all the characteristics required to follow the same path.

In 2007 a number of European key players in the field of Photonic Integration Technology, cooperating in the JePPIX technology platform, introduced a generic foundry model, using highly standardized integration processes that can be used in a broad range of different applications, similar to the approach in microelectronics. Such processes bring a number of important advantages:

• By sharing the process between many users the advantage of scale (low fabrication cost) can be reached at much smaller volumes per user.
• By using a standardized generic process, a number of designs can be combined in a single fabrication run, a so-called Multi-Project Wafer (MPW) run. It reduces the costs of a small set of test chips by more than an order of magnitude and it brings PIC development within reach for small and medium sized enterprises (SMEs) and other innovative research groups with modest budgets at their disposal.
• Using generic processes, the qualification costs for a product are also greatly reduced, because the process itself is qualified, so that the PIC qualification can be restricted to specific product features.

Presently a number of large R&D projects are running, developing both the generic foundry technologies and the infrastructure to make them accessible at low cost for a broad range of companies: design tools, component libraries, generic packaging technology and generic test facilities. This model, in which Europe is clearly leading, will bring Application Specific Photonic ICs (ASPICs) within reach for many SMEs and larger companies for which the entry costs of today’s technology are too high. In the coming years Generic Integration Technology is going to cause a revolution in the application of Photonic ICs, similar to what happened in microelectronics thirty years ago.

A recent report estimates the global photonics market in 2015 at 450 B€, i.e. about 1/5th the size of the electronics market. If the photonic integration market is going to take a share of only a few percent (in comparison: microelectronics takes about 15% of the total electronics market) it will become a multi-billion market and enable an applications market that is many times larger.

In the present report, a roadmap for the development of generic photonic foundry technology based on InP and dielectric $Si_{3}N_{4}/SiO_{2}$ (TriPleX) technology is presented. Since the publication of the previous roadmap in 2013 significant progress has been made. In 2014 all four JePPIX foundries (Oclaro, Fraunhofer HHI, SMART Photonics and LioniX) have been offering semi-commercial access to MPW runs in their generic integration processes, and the interest in participation in experimental foundry runs is growing significantly faster than we anticipated back in 2011 when the first JePPIX roadmap was published. Based on these developments we remain confident in our earlier predictions of a >1 B€ ASPIC enabled market by 2020.

1 JePPIX: Joint European Platform for Photonic Integration of Components and Circuits. See Chapter 11.
2. Applications

The anticipated large reduction in R&D time and chip manufacturing costs will lead to a large growth in the share of Photonic ICs in the photonic components market. So far the use of PICs has been mainly restricted to applications in the telecom core-network, where their specific functionality cannot be met by competing technologies.

As many more companies can profit from low-cost access to fabrication of Photonic Integrated Circuits using generic foundries, this opens up a whole new range of applications, including data communications, fibre-to-the-home, fibre sensors, gas sensing, medical diagnostics, metrology and consumer photonics.

In the framework of the EU projects EuroPIC and PARADIGM, and the Dutch MEMPHIS project, a large number of Application Specific Photonic ICs have been developed and tested. More than 250 designs have already been processed on the foundry platforms, of which many are for industrial and project-external users. Examples of some of them are shown in Figure 1 on the next page.

The open access foundry model is particularly important for SMEs; it provides them with access to this high tech field with relatively low entrance costs. We expect that the foundry model will first be adopted for fields that are presently attractive for SMEs. Examples are the markets for fibre sensing equipment, medical diagnostics methods like Optical Coherence Tomography (OCT), photonic beam steering and metrology. But also in telecommunications and data communications it will become important especially for applications that require advanced functionality. Here the shortened R&D time achieved using generic processes will provide the foundry approach with a competitive advantage.

We foresee also interesting developments through combination of InP and TriPleX platform capabilities. As mentioned in Section 4 research is underway to enable low-cost precision co-assembly of InP and TriPleX chips which will bring us a hybrid platform technology in which we can combine the active functionality and high-speed operation of InP technology with the record low-loss capabilities of the TriPleX platform.

Whilst we expect that the foundry model will begin by penetrating small to medium volume markets, we expect it to become competitive in high-volume markets in due course because of the steady increase in capability and performance that is anticipated.

Pim Kat  
(CEO Technobis group)  
TFT-FOS has made a tremendous step forward in the development of dedicated FBG interrogator systems. Three of our basic InP ASPIC designs have been adopted by large OEM customers and two of them will result in commercial products this year. The opportunity of experimenting in JePPIX/PARADIGM and the support of the Bright Photonics designer helped us to create a lot of new business.

Mark Thompson  
(Quantum Photonics - University of Bristol)  
As a University research group, it is essential that we work at the cutting edge of science, engineering and technology. The multi-project wafer approach of JePPIX / Paradigm makes this possible by enabling affordable access to state-of-the-art photonic device fabrication facilities that would otherwise be prohibitively expensive and out of the reach of typical academic research. This approach has allowed us to develop prototype device concepts in the emerging field of quantum communications.

Gerlas van den Hoven  
(CEO Genexis)  
Fibre-to-the-home will be one of the major infrastructure investments of the 21st century, providing end-user access to the digital highway. The role of photonics is crucial to enabling this. The challenges are cost, power consumption and density; and the key to solving those challenges lies in nano photonics and photonic integration. It is exactly these themes that the JePPIX roadmap addresses.
Figure 1  Examples of ASPICs realized in MPW runs and their applications.
The ecosystem for Photonic ICs
Successful introduction of a novel technology requires a close interaction between the users and the providers of that novel technology. JePPIX has been extremely successful in bringing together the key players in the field of photonic integration. The eco-system is depicted in Figure 2.

The largest group, both in number and market volume, is formed by companies using Photonic ICs in improved or novel products. Many of them are SMEs without the expertise to design a chip themselves.

The second group are PIC designers and software vendors. PIC designers form the bridge between the users and the foundries by translating the functional requirements of the users into a PIC design that can be produced in the foundry. The software vendors develop and provide the necessary tools to simulate the circuits and create the required mask layouts. The work that is done on the development of mature design kits to bridge the gap between the foundry and the designer plays an especially important role in the evolution of the JePPIX eco-system.

The third group are the enablers for this market, the generic foundries that provide cost-effective access to their high-performance technology, and the companies providing low-cost packaging and testing for the chips.

A fourth key group are the providers of R&D in all three sectors. This R&D drives a dynamic similar to Moore’s law in electronics by developing new generations of foundry technology and new equipment with ever increasing performance, increasingly powerful design software, component and sub-circuit libraries, and by developing advanced Application Specific Photonic ICs (ASPICs) for novel or improved user applications.

The business cases for the different groups are very different, we will discuss them below.

The business case for PIC users
For companies that are manufacturing or developing photonic products, Photonic ICs will bring major advantages:

- Integration of a subsystem consisting of a number of individual components, such as lasers, modulators, detectors, couplers and filters, will reduce the overall manufacturing costs, including the bill of materials, by an order of magnitude, because only one chip has to be packaged instead of a number of discrete components. In cases where the packaging costs are dominant, the cost of the packaged integrated circuit will be much lower than the cost of the separate packaged components.

- The elimination of a lot of fibre-chip coupling and packaging leads to a better optical and mechanical stability of the sub-system, lower power consumption (less Peltier cooling) and a much smaller form factor.

- While the above mentioned advantages are common to all integration models, the generic foundry model brings the low-cost advantage already at much lower volumes, because of the cost sharing inherent to the approach. Further, through the use of MPW runs, it offers the additional advantage of low entry costs, which make it affordable particularly for SMEs and exploratory design projects.

The situation is comparable with the situation in microelectronics in the seventies, where integrated circuits replaced discrete circuits in most applications. Examples of photonic ICs that may replace existing equipment are PICs for telecoms and datacoms applications, for application in fibre sensor readout units, and for use in medical diagnostics and metrology. In the former field, the US company Infinera is a prominent example of how PICs can revolutionize business strategy.
The higher complexity that is possible in PICs and the short and stable interconnections, allow new functionalities, for example a whole range of phase sensitive functions which cannot be realized with sufficient stability in fibre-based systems. This will give rise to novel products with functionalities that are presently not practically feasible. For such novel applications the business case will have more uncertainties about the market.

We expect that the combined advantages of lower cost, smaller form factor, greater stability and lower power consumption will provide a promising business case for a large number of companies, as soon as qualified foundry processes become commercially available.

The business case for PIC designers and software vendors
In microelectronics IC designers and design houses form a large group, much larger than the number of people involved in IC fabrication. In Photonics the number of experienced PIC designers is today very small. We expect that the demand for PIC designers will increase rapidly when qualified commercial processes become available. Many OEMs and end-users will not choose to hire and train ASPIC designers within their own company when first starting out with ASPICs. We are already seeing specialist design houses established to work with fabless and labless SMEs and companies. Starting your own PIC design company is an interesting option for PhD students educated in the field since the capital investments required are relatively low, mainly in software licenses. The availability of a broad group of PIC designers will give a large boost to the development of the field, and will create a business sector with a significant amount of high-tech employment. In addition the adoption of the application of photonic integration technologies is bringing additional business to the software vendors involved in supplying design solutions for this market. Vendors are reporting double digit growth numbers over the last couple of years, and it is expected that this will further increase as a result of the accelerated pick-up by industry now that the generic processes are becoming available in (semi) commercial offers. Foundries and software vendors will need to work together and invest in process design kit (PDK) development.

The business case for PIC foundries
The PIC foundries are the enablers of a business sector that promises to become very large, even though it is difficult to quantify at this stage. Their business case must take a long term view, however. They need to make large investments upfront in developing qualified, high-performance foundry processes. TSMC, the world's largest microelectronics foundry, proves that foundries can be profitable, but they need large volumes to generate sufficient return on their investments. In the starting phase of the foundry approach, which may take several years, it will be difficult for the foundries to survive on pure generic foundry business alone. Successful business models may include smaller pure-play foundries through to larger integrated device manufacturers (IDMs) offering a service to external users as is done in the electronic IC sector. The former offers an independence which may be valuable to some customers, while the latter has a proven path to volume production.
As open access foundries serve as a kind of public service infrastructure that supports an important business sector, it is logical that in the starting phase public support is also provided to make the business sufficiently robust through risk sharing and market stimulation. We will discuss this in more detail in the R&D investment roadmap.

The business case for JePPIX
A central organisation is crucial for effective coordination of the whole eco-system. JePPIX is playing such a role by addressing the following tasks:

- Brokering: combining designs from different users in Multi-Project Wafer (MPW) runs. In this way the costs of R&D runs can be shared by many users, which leads to a dramatic reduction of the entry costs.
- Organising proper documentation and training for the available foundry processes.
- Reaching out to potential users and mentoring through the decision process and design-fab-test flow, identifying opportunities that the novel technology brings for their product portfolio. Bringing them into contact with designers with expertise in their field.
- Setting the strategic roadmap and providing leadership in this new technology sector.

We are confident that in a few years the costs of JePPIX can be covered by a simple fee charged for its services in a similar way as for MOSIS\(^5\) and Europractice\(^6\).

\(^5\) [www.mosis.com](http://www.mosis.com)
\(^6\) [www.europractice.com](http://www.europractice.com)

As a result of significant investments in the development of foundry technology infrastructure (well over 50 M€ in European and national projects so far) Europe is making substantial progress in this new way of working. In this section we give an overview of the present status of the foundry capabilities of the JePPIX partners and a prediction for the status in 2016, 2018 and 2020.

History
In 2007 the COBRA institute at TU Eindhoven started pioneering small scale foundry access to a first generation research platform in the framework of the EU-FP6 Network of Excellence ePIXnet using its own cleanroom facilities and know-how. Process capabilities have been gradually improved and presently support design of ASPICs integrating lasers, optical amplifiers, modulators and detectors with 10 Gbits/s speed, and a variety of passive optical components. In 2009 the FP7 EuroPIC project began with the mission of transferring the foundry model from a university environment into industrial platforms (the wafer fabs of Oclaro in the UK and Fraunhofer-HHI in Germany) and started development of process design kits (PDK) and standardized packaging solutions. EuroPIC successfully pioneered the world’s first photonic MPW-runs in generic industrial foundry processes in 2012. Oclaro tested a transmitter type platform offering a variety of lasers and optical amplifiers, modulators and detectors for 10 Gbits/s operation and passive building blocks like MMI-couplers and AWGs. Fraunhofer HHI tested a receiver type platform offering detectors for operation up to 40 Gbits/s, integrated with a variety of passive devices and thermo-optic phase modulators. The COBRA process was licensed to the spin-off company SMART Photonics, providing the first pure-play foundry services for ASPICs.
LioniX started developing its TriPleX technology for low-loss dielectric waveguide devices and circuits in 2004. First devices focused on microwave photonics applications, but over the last ten years the technology has been developed into a very advanced platform appropriate for a broad range of applications covering a wide wavelength range - from the visible to the infrared.

Present situation 2014
Since 2014 all four JePPIX foundries have been offering semi-commercial access to early versions of their foundry processes. The capabilities of the platforms are briefly summarized below.

**The Oclaro platform** offers optical amplifiers, rf modulators, detectors, tunable Bragg gratings, Spot-Size Converters (SSCs) and a variety of passive components including MMI couplers and AWGs. The SOAs provide about 50 cm\(^{-1}\) gain over the whole C-band and can deliver 50 mW output power in the output waveguide. The rf modulators support 10 Gbits/s modulation with 3.5 V modulation voltage, for a modulator length of under 1 mm. The detectors have a responsivity of 0.7 A/W and a 10 GHz bandwidth. Tunable Bragg gratings support tuning over 7-8 nm. The Spot Size Converters (SSCs) with a 3 μm spot diameter provide coupling to lensed fibres with 1-2 dB coupling loss. The waveguide propagation loss is about 3 dB/cm. Typical insertion losses for MMI optical splitters and AWG de/multiplexers are 1 dB and 3 dB, respectively.

**The HHI platform**, starting as a “receiver-only” platform, offers very high-speed photodetectors, SSCs, thermo-optic phase modulators and a variety of passive waveguide components. The rf detectors exhibit an internal responsivity of 0.9 A/W, a dark current <10 nA and an electro-optical bandwidth of 40 GHz. SSCs provide 1.5 dB coupling loss to a cleaved Standard Single Mode Fibre. Waveguide propagation loss varies between <1 dB/cm for low-contrast waveguides to some 2 dB/cm for high-contrast waveguides. MMI couplers and AWG de/multiplexers have typical losses of 0.5-1 dB and 2-3 dB, respectively.

**The SMART Photonics platform** offers optical amplifiers, rf modulators, detectors and a variety of passive components. The SOAs provide about 50 cm\(^{-1}\) gain and 20 mW output power. The rf modulators support 10 Gbits/s modulation with 5 V drive voltage for 2 mm long phase modulators. Detectors have 0.8 A/W responsivity and >20 GHz bandwidth. Waveguide propagation losses are 2-3 dB/cm.

**The TriPleX platform** offers low-loss straight waveguides, bends, S-bends, offsets, splitters, spot size converters, lateral tapers and thermo-optic phase shifters. Combinations of these building blocks allow, for example, the creation of microwave photonics ASPICs through combinations of Mach-Zehnders and micro ring resonators. The current platform has guaranteed losses below 0.5 dB/cm and results reported by customers have been as low as 0.1 dB/cm.
Technology Roadmap

Roadmap 2016
In 2016 the following extensions and improvements for the platforms are foreseen. All platforms will offer a basic level of platform qualification, including some early yield figures. In addition to the process development activities, work will commence to improve the contents of the PDKs.

The Oclaro platform will provide transmit and receive capabilities (modulators and detectors) for operation at 40 Gbits/s. Modulators will operate at 40 Gbits/s with 3.5 V drive voltage. Detectors have 0.9 A/W responsivity.

The HHI platform will add transmitter capabilities to its current receiver platform: SOAs, DFB/DBR lasers and EAMs. Further, it will add Polarisation Converters, thus providing the platform with polarisation handling capabilities. The platform will support 25 Gbits/s modulation, either by direct modulation of the DFB lasers or using Electro-Absorption Modulators.

The SMART Photonics platform will offer less than 1 dB/cm waveguide propagation loss and support 100 nm device features (using 193 nm DUV scanner lithography), which will lead to enhanced performance and reduced insertion loss of passive components. Further, it will add Spot Size Converters and improve the efficiency of its detectors and modulators.

The TriPleX platform will add more advanced building blocks to its current library. Structures like AWGs and micro ring resonators are on the roadmap of LioniX for implementation in the platform. It is also foreseen that the guaranteed loss will be lowered close to the best-case reported value of 0.1 dB/cm and that low power phase tuning will be introduced.

Roadmap 2018
In 2018 all platforms will offer an extended level of platform qualification, including yield and lifetime figures. All platforms will offer low loss waveguides (<1 dB/cm), efficient SOAs, modulators and detectors, polarisation converters and spot-size converters and provide a performance comparable to the state-of-the-art application specific processes available on the market.

The TriPleX platform will offer integrated MEMS structures that enable, for example, low-cost high-precision coupling between InP and TriPleX PICs, thus providing a hybrid platform that combines the best of InP and TriPleX technology; high performance active devices and very low-loss and high-Q passive functionality.

The COBRA research platform. In 2010, research started on the InP Membrane on Silicon technology (IMOS). This approach will make it possible to fabricate InP photonic ICs on 200 or even 300 mm silicon wafers. In 2015 we started research on wafer scale integration of InP photonics and BiCMOS electronics, first demonstrators are expected in 2018. Small scale experimental access would follow shortly after. The intimate integration of high-speed electronics, digital electronics and photonic ICs in the same chip will have a profound impact on module costs and performance.

Roadmap 2020
In addition to high-performance photonic technologies, R&D-level MPW runs will be offered that combine wafer-scale photonic/electronic integration processes. In these processes, the full functionality of photonic platforms will be provided on top of (Bi)CMOS ICs in which the driver, receiver and control electronics are integrated.
The potential of a foundry process is, to a large extent, determined by the maturity of the technology reflected in the contents of the Process Design Kit provided to its users. Such a PDK is compatible with design software and contains in general:

- Technology set-up files, describing the mask layers involved in the fabrication process,
- Pre-defined mask layouts and specifications for a set of Basic Building Blocks,
- Mask layout and accurate models for a variety of more complex components,
- Design and verification rules.

**Present situation 2014**

All four JePPIX foundries have a process design kit containing a component library providing the mask layout for Basic Building Blocks and the most commonly used Composite Building Blocks, such as MMI splitters and AWG de/multiplexers. In the accompanying Design Manual, some numbers on component performance are given, but the specification is not yet complete and no statistics are provided. Some design rules are checked by the mask layout software, but at a very basic level.

In the past two years altogether more than 200 designs have been fabricated using these process design kits, in the projects EuroPIC, PARADIGM and Memphis as well as in commercial activities.

**Roadmap 2016**

To obtain more mature PDKs, activities will be undertaken to further stabilise the process performance and to collect in-line and off-line measurement data from the fabrication processes and test structures. This work will drive the compact model development for the components in the libraries, enabling the ability to simulate more complex Photonic Integrated Circuits, based on accurate models.

Furthermore the number of design rules that are incorporated in the design kits will be increased in number and sophistication to reduce the design errors which may hamper fabrication and/or performance of the circuits.

Due to the open nature of the design eco-system centred on the PDAFlow API (see [www.pdaflow.org](http://www.pdaflow.org)), we expect more software vendors to engage and provide design solutions compatible with the JePPIX PDKs. In addition design modules or intellectual property (IP)-blocks from external parties like design houses, universities or software vendors will start appearing. These will be built on information provided by the foundries in the PDKs.

Furthermore the packaging options for test and low-volume fabrication will be incorporated in packaging templates, to enable design for packaging strategies.

**Roadmap 2018**

We expect that in 2018 for all the Basic Building Blocks library modules will be available that provide mask layout, accurate component specifications and model descriptions including statistical data to enable application specific tolerance studies. Further, parameterized library modules with simulation models including statistics will be available for a number of frequently used components, like AWGs, MMI-couplers, pulse lasers and tunable CW lasers, rf modulators and detectors. The Design Rule Checkers will have achieved a performance level in which not only are the most common design errors automatically detected, but also warnings given for layouts likely to compromise good circuit performance.

**Roadmap 2020**

In 2020 we expect the contents and the performance of the PDKs to have further improved. An important novel feature will be the offering of library models for a number of electronic circuits, like drivers and receivers complete with interconnection circuits. Activities on the alignment of the photonics standards with existing initiatives in electronics design standardisation will be undertaken; allowing for better integration of electronics and photonics.

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**5. Process Design Kit Roadmap**
The rapid developments in generic integration technology have led to a dramatic reduction of the cost of PIC development and manufacturing at low and medium volumes. This has not yet been followed by a similar development in the cost of packaging and testing, however. For many applications these costs could be significantly higher than the cost of the chip. Therefore, development of generic packaging and testing methods has high priority. The key to such a generic approach is the definition of standards for the form factor and the position of optical and electrical (dc and rf) output ports.

Generic packages are most important for R&D, prototyping and low volumes. For special applications and high volume production, they may serve as a starting point, but they will have to be further optimized. For R&D, prototyping and low volumes JePPIX is working on a standard for two generic packages:

1. A low cost test assembly which has fibres and electrical leads connected to the chip (< 500 € for a single package). This package is suitable for chip testing but not for commercial applications.
2. A medium cost high-performance package (target: 1000 € for packaging a single chip, 100-200 € per package for larger volumes). This package will accommodate up to 10 optical ports, 10 rf ports (25 GHz) and > 30 dc ports. From a performance point of view this package is suitable for commercial applications. We expect that a packaging service will be offered via JePPIX starting 2017.

For these standards a template is available in the PDKs, so that designers using this template can be sure that it will fit the generic package. The standard is parameterized and complies with a small set of different chip dimensions (form factor) and a different number of optical and electrical ports.

With these generic packaging standards and the templates provided through the PDKs, application specific requirements for the PIC can be addressed while enabling a design for packaging strategy.

Interested companies are advised to contact JePPIX (coordinator@jeppix.eu).

For chips that are designed with the generic packaging templates in the PDKs we are developing standardized test setups. We expect that starting in 2017 open access to high-performance test facilities can be provided via JePPIX. Further, we are jointly developing generic and semi-automatic equipment for on-wafer testing and chip validation with the foundries that will lead to a significant cost reduction for qualification and testing. The first pieces of such equipment should also become available in 2017.

7 Linkra S.r.l., www.linkra.it
For application of photonic ICs in new or improved products the following costs have to be distinguished and will be briefly described below:

- Prototype development costs,
- Chip manufacturing costs,
- Cost of packaging and testing.

**Prototype development cost**

For developing a prototype of an ASPIC the main costs are in the design, the participation in one or more MPW runs in order to get a prototype on specs, and the characterisation and testing.

The design costs are mainly salary costs of the designer; they can be significantly reduced by the availability of dedicated Process Design Kits which contain a library with layout and simulation modules for the basic components in the foundry process and software for automatic Design Rule Checking (DRC). Design time is strongly dependent on the complexity of the design and the experience of the designer. Typically it is between a few weeks and several months. In due course the accuracy and the number of the components and sub-circuits supported by the libraries will grow and the design time will reduce accordingly. Eventually first-time-right designs will become feasible for designs that are well within the design rules.

The price for participation in an MPW run is mainly determined by the design area of the chip. For the foundry processes available through the JePPIX platform the costs for fabricating an ASPIC design in an InP MPW run vary at present between 300 \( \text{€/mm}^2 \) design area for the simplest process up to about 1000 \( \text{€/mm}^2 \) for the most complex one. Square millimetre cost for an ASPIC design in a TriPleX MPW run are 63 \( \text{€/mm}^2 \), and as low as 33 \( \text{€/mm}^2 \) for academic users.

For these amount the user will receive 8 copies of an InP ASPIC, or 4 copies in the case of a TriPleX ASPIC. Table 1 shows a price-performance comparison between MPW participation fees for a number of InP, TriPleX and silicon photonics foundries.

A set of small chips in a simple process may thus cost less than 5000 \( € \) in an InP MPW run. For the 100-channel spectrometer chip shown in Figure 1 top right, which integrates 100 detectors with 11 AWGs on a chip area of 6x8 mm\(^2\), the cost for participation in an MPW run will come to about 11,000 \( € \) including some overhead for brokering services. The numbers in Table 1 are a snapshot from the situation in 2014 and can be subject to change.

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### Table 1

<table>
<thead>
<tr>
<th>Broker</th>
<th>Process</th>
<th>Lasers</th>
<th>SOAs</th>
<th>TRS</th>
<th>Modulators / Phase shifters</th>
<th>Detectors</th>
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<td>YES</td>
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<td>YES</td>
<td>1.35</td>
<td>&lt; 2</td>
<td>&gt; 10</td>
<td>0.8</td>
<td>10</td>
</tr>
<tr>
<td>JePPIX HHI Rx 40</td>
<td>0.5 (25 mW)</td>
<td>&lt; 2</td>
<td>(kHz)</td>
<td>0.8</td>
<td>40</td>
<td>&lt; 10</td>
<td>1-2</td>
<td>3 x 6</td>
<td>€5,500</td>
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<td>JePPIX SMART TxBx10</td>
<td>YES</td>
<td>YES</td>
<td>2</td>
<td>7</td>
<td>&lt; 2</td>
<td>10</td>
<td>0.8</td>
<td>10</td>
<td>&lt; 20</td>
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<tr>
<td>JePPIX TriPlex (DS-500-170)</td>
<td>1.2</td>
<td>(500 mW)</td>
<td>&lt; 0.1</td>
<td>(kHz)</td>
<td>&lt; 0.5</td>
<td>16 x 16</td>
<td>€16,000</td>
<td>63</td>
<td>4</td>
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<tr>
<td>ePIXfab imec ISIPP25G</td>
<td>1.5</td>
<td>8.5</td>
<td>5</td>
<td>11</td>
<td>0.5</td>
<td>&gt; 50</td>
<td>&lt; 50</td>
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</tr>
<tr>
<td>OPSIS 5</td>
<td>3</td>
<td>9</td>
<td>5</td>
<td>30</td>
<td>0.7</td>
<td>&gt; 50</td>
<td>3300</td>
<td>1-2</td>
<td>2.5 x 2.5</td>
</tr>
</tbody>
</table>

Footnotes: 1 universities get 45% reduction on TriPleX MPWs, 2 OPSIS stopped brokering service in 2014.
Cost Roadmap

Chip cost in volume production
Scaling laws for InP and TriPleX are similar to other thin film fabrication technologies like CMOS electronics or silicon photonics, so with increased wafer size and throughput of the fab the square millimetre price will steadily decrease. Figure 5 shows how the square millimetre cost of InP PICs depends on the load of the fab, for different fab scenarios. The load of the fab is expressed in the number of chips/year for an average chip size of 20 mm². For smaller chips the curves will shift to the right, for larger chips to the left. The first three scenarios are for small InP wafer fabs for handling 75, 100 and 150 mm wafers, respectively. The forth scenario is for a small 200 mm fab, in which an InP photonic layer is integrated on a 200 mm silicon substrate, as in the IMOS technology mentioned in the technology roadmap (section 4). From the figure we see that for larger fabs the starting costs will be higher, so that higher volumes will be needed to arrive at low square millimetre costs.

The graphs are indicative of real chip prices, but they can differ significantly for different implementations\(^9\); e.g. whether the fab is highly automated or not, and at the high volume end the process costs will be dependent on the complexity of the manufacturing process. Further, yield and profit margin have been introduced in a simple manner. Yield is a more difficult parameter to include since there is an inherent, market driven trade-off between the requirements that the users place on the Building Blocks (BBs) and the specifications offered by the fab. Tight specs will reduce yield, but the general conclusions are not very sensitive to these effects, fundamentally being driven by fab capital cost and chip volume.

Keeping all these reservations in mind we can draw a few conclusions from the graph.

- The figure illustrates the advantage of the foundry model: because the square millimetre costs are strongly dependent on the total volume, all users of the fab can get their chips at the price corresponding to the total yearly chip volume, while their own chip volume may be much smaller. This will make the costs for small users significantly lower.
- For a square millimetre price below 10 €/mm\(^2\), volumes over 100,000 chips per year are required. This comes to about 1000 75-mm wafers, which can well be handled by smaller fabs.
- For a square millimetre price below 1 €/mm\(^2\), volumes well over 1 million chips per year are required.
- An important conclusion is that at low up to medium volumes large fabs will be more expensive because of the higher investments which pay back only at larger volumes. For a 200 mm fab, for example, chip volumes of several millions/year are required to make it competitive to smaller fabs. In a starting phase, in which the total chip volumes for a foundry will start at numbers well below 1 million chips per year, smaller fabs offer lower cost.

Example: at a 10 €/mm\(^2\) level the cost of the InP-based spectrometer chip described above, which integrates 100 detectors with 11 AWGs on a single chip, would be in the order of 500 €. If the foundry volumes increase we expect that the cost can go down below 100 €, also for small volumes. This is very competitive with non-integrated technologies. For the TriPleX process chip costs will be even lower: the square millimetre costs can go down below 2 €/mm\(^2\), but the chip dimensions will typically be larger than for InP ASPICs.

\(^9\) Details of the model are available from JePPIX.
Packaging and testing cost
Another important cost factor is the packaging of the chip. With the current state of the packaging technology it will be significantly higher than the cost of the chips. The JePPIX consortium is, therefore, working on a small set of standardized generic packages for a broad class of different chips with standardized positions of the optical and electrical input and output ports, as described in the Packaging and Testing roadmap section. The cost of generic packages should reduce ultimately to a few hundred euros for small volumes of high-performance chips with a significant number of optical and RF ports, and something in the order of a few tens of Euros for large volumes of simple chips. For very high volumes application specific packages will be even cheaper.

For reducing the cost of testing, development of automated on-wafer test facilities is of key importance. In the PARADIGM project first steps into this direction have been taken and open access to standardized or dedicated high-end test facilities for R&D purposes is on the JePPIX roadmap. Open access to test labs will enable lab-less or insufficiently equipped users to assess their prototypes in an early stage without the need for high investments in dedicated test equipment.

Comparison between InP and Silicon Photonics
The most important qualities when comparing InP and Silicon Photonics PICs are functionality, performance and cost.

Functionality and performance
The fundamental and key advantage brought by InP is the ability to monolithically integrate compact and efficient optical amplifiers. Optical amplifiers play a comparable role in photonics to that of transistors in electronics. They are at the heart of any laser or laser system, but they are also used in many other applications, like switching, broadcast, wavelength conversion, power level control etc. Without efficient integration of optical amplifiers the road to large scale integration is blocked: it is impossible to provide large scale photonic ICs with sufficient amplifiers in a hybrid way. That’s why InP-based photonic ICs are clearly leading in circuit complexity.10

Cost
For the cost of integrated photonics solutions it is important to distinguish between chip cost and module cost. In many applications, particularly those requiring multiple optical and rf connections, the cost of the chip is only a small part of the total cost of a module, because the assembly and packaging costs are dominant. The technology that can integrate most functionality into a single chip will lead to the largest reduction of the costs of assembly and packaging and the associated loss in performance. So even if the InP chip is more expensive, the cost of the InP-based module will be lower, and its performance higher.

Cost Roadmap

It is questionable, however, whether InP chips are really more expensive than silicon photonics chips. Here we have to distinguish between small to medium volume markets and high volume markets. From the analysis in the previous paragraphs we see that due to the large scale of its fabs and the associated high investments, silicon photonics is not well positioned to serve small and medium sized markets and InP-fabs have a better offer, both in terms of functionality and price. The dashed line (200 mm fab) in Figure 5 (chip cost) can be considered representative for a small silicon photonics fab. We see that volumes well over one million chips per year are required to make such a fab competitive with respect to chip cost, and for larger fabs even larger volumes are required.

For very large markets silicon photonics is better positioned than for smaller markets, but as can be seen from Figure 5 the same holds for InP: if the wafer size and the fab size is scaled up, the chip cost will go down in a similar way as for silicon photonics, whereas at the same time, the performance remains better. The contribution of the material costs (InP or Si) to the total chip cost is negligible. The chip cost is determined by the cost of the processing, and this is dependent on the size of the wafers and the size of the fab. A point of concern may be the wafer size, which is presently limited to 6” for InP. However, research is also going on for heterogeneous integration of a fully InP-based photonic layer on silicon (IMOS). We may speculate that such a technology could bridge the present gap between InP and silicon-based photonics, and may prove a faster track to wafer scale integration of photonics and electronics than via hybrid integration of InP and silicon photonics.

In summary: The wide-spread believe that InP photonics is much more expensive than silicon photonics is highly erroneous. Not only does InP offer significant performance advantages, but, for the short and medium term, InP-based photonic integration offers clear cost advantages over silicon photonics as well.

8. Market Roadmap

InP-based PICs are now entering the marketplace. An early example was the 100 Gbits/s transmitter PIC from the company Infinera. With the introduction of advanced modulation formats in 100+ Gbits/s data links commercial application of InP PICs will rapidly increase. The market for other applications is still small. We expect; however, that due to the dramatic reduction of R&D and prototyping costs in the generic foundry model, the market for PICs fabricated in generic foundries will rapidly increase.

R&D prototypes

In the JePPIX 2012 Roadmap we published our first market prediction for generic InP PICs. The model was based on the development of the number of R&D prototypes fabricated in InP-based MPW runs. It included some assumptions about the fraction of the prototypes that would make it into a commercial product, and the growth of the market for those products. The details are explained in the 2012 and 2013 roadmap.

Figure 7 shows the graph that we published early 2012. The coloured bars for the years 2012 and following indicate our predictions for the total number of InP ASPIC designs in MPW runs. The bars labelled “update 2015” indicate the real numbers. As can be seen the numbers of ASPIC designs have grown significantly faster than we predicted in 2011. In 2014 we started offering semi-commercial access and we reduced the free access, which has led to a reduction of the number of university designs. However, as can be seen from Figure 8 the number of ASPIC designs for companies is growing fast, which is an important step towards commercial exploitation. Even though the number of university designs has decreased now that the access is no longer free, the university interest in semi-commercial access is still significant.

The guiding model for our market and investment roadmap is the very successful MOSIS programme that has made silicon VLSI technology accessible to a broad community in the US; since 1981 more than 50,000 IC designs have been processed through the service. MOSIS has pioneered training and access to VLSI technology through MPW runs. In its first phase MOSIS provided free access for universities to a number of silicon foundry processes. This provided the program with a huge leverage; it attracted a large number of PhD students and other designers whose salaries were paid from other sources. A significant number of these designs have led to very successful products and companies and given a large boost to the development of VLSI technology as a whole.

As mentioned in the introduction a German market report (2013) predicts a Photonics market exceeding 600 B€ in 2020, divided over nine different sectors:\footnote{12} Production technology (7%), Measurement and Automated Vision (9%), Optical Components & Systems (6%), Safety & Defence Technologies (7%), Medical Technology & Life Sciences (7%), Communication Technology (4%), Information Technology (15%), Displays (23%), Light Sources (6%) and Solar cells (16%). We expect that Photonic ICs will be applied in most of these sectors, except perhaps the last three. Even if the market for PICs becomes only a few percent of this total market (in comparison: the share of nano and microelectronics technology in the total electronics market is about 15%) it will become a multi-billion euro market, and crucially it will enable a far larger applications market.

\footnote{11} ITEM: Innovation Technology Entrepreneurship & Marketing Group, www.item-eindhoven.nl

\footnote{12} Optech Consulting, Studie ”Photonik 2013”, in: Spectaris, VDMA, ZVEI, BBF, “Branchenreport Photonik 2013”.

Market Roadmap

![Figure 7](image.png)

**Figure 7** Development of the applications market enabled by ASPICs. The bars from 2012 indicate our predictions, made in 2011. The bars labelled ‘update 2015’ indicate the actual development.

![Figure 8](image.png)

**Figure 8** Number of ASPICs developed on foundry platforms, differentiated for designers from universities, companies and research institutes.

### Commercial exploitation

The increased interest of companies in ASPIC prototype development is an important step towards commercial application. In our 2012 roadmap we predicted that the market of products enabled by ASPICs will take off after 2014 and exceed 1 B€ before 2020. Based on the recent developments as indicated in Figures 7 and 8 we are confident that these predictions will prove realistic. A more detailed analysis of barriers and needs to introduce photonic ASICs into company business, based on opportunities and challenges created by photonics for ASPIC enabled products and services, is presently being undertaken by the ITEM group of TU/e\footnote{11}.
Public funding is essential to provide stability and continuity to new services and new technologies in the early development phase, just as DARPA funding in the US established the MOSIS programme in its early years. With increasing maturity, costs must increasingly be spread through private investment in new products and applications in a synergistic partnership between public support for access projects and commercial investment. How this partnership could evolve for each of the main stakeholder groups is discussed here.

PIC Users

Through the generic foundry model the required investment level for applying PICs in novel or improved products is within reach for many SMEs and the participation fees for MPW runs can fit the budget of almost any small sized research project. For introducing PIC-based products on the market it is important that companies can get easy access to investment capital, which is still a matter of concern in Europe.

From the 5000 entries listed by the European Photonics Industry Consortium EPIC\(^\text{13}\) as companies working with Photonics, many may become PIC users, but only a few of them are presently aware of the benefits that photonic ICs will bring them. Therefore, the focus of public funding for the user community should be on raising awareness among companies and providing low-cost access to universities in order to explore the potential of photonic integration, similar to what MOSIS and Europractice do for microelectronics.

A recent US report\(^\text{14}\) recommends the application of the same model to photonics foundries. In Europe the EU ACTPHAST project has started a similar program, providing SMEs with free access to a range of photonic technologies for first prototype trials (larger companies have to contribute 50% of the cost). For universities there is no such programme yet in Europe which from the JePPIX perspective seems to be a significant omission. To increase awareness about the opportunities of photonic integration among industrial companies we recommend the following actions:

- **Awareness**: Programs to reach out to SMEs, making them aware of the opportunities that photonic ICs can bring them, and offering assistance for trying out ASPICs. The ACTPHAST project is presently offering a prototyping service, but with the present approach only a few tens of companies can be served by this project. Investments in scouting to reach out to a large number of the 5000 companies in Europe that use photonics, should be increased. Such programs should also include some effort on analysis of existing and novel markets.

- **Support**: Establish centres of excellence for ASPIC design and testing in various European countries that can reach out to new users and assist them in getting familiar with PICs or finding a professional designer or application developer, and characterisation and test facilities.

- **Incentives**: Programs designed to provide low cost access to universities. Many PhD students will be interested in designing on advanced foundry processes. This will provide a huge leverage for PIC-based innovation because it will direct funding from existing programs towards PIC-based research. A number of these PhD designs will surely lead to commercial products or start-ups. The approach is similar to the early MOSIS program in the US.

PIC designers

The number of experienced PIC designers in Europe is still very small, just a handful. With the rapidly increasing demand predicted in the analysis of Figure 7 we expect this to become a major bottleneck in the expansion of the field. At present the market in which PIC designers operate is at an early stage of development. It is still difficult for PIC designers and design companies to make a full time business out of it, so many PhD students with good skills in PIC design leave the field after their PhD.

\(^ {13}\) EPIC: European Photonic Industry Consortium, [www.epic-assoc.org](http://www.epic-assoc.org)

\(^ {14}\) IDA Report on Photonics Foundry Ecosystem, April 2014
To retain design expertise it is important that the institutional frameworks of Universities and research institutes facilitate combinations of a research position with a part-time job in a design company. In this way we can build more design capability, which can be exploited in a flexible manner by companies and R&D groups. Having available a large pool of designers will strongly accelerate the introduction of photonic ICs because such designers will build their own networks and start active scouting leading to increased awareness amongst potential customers.

**Testing of PICs**

Test is another important area driving cost and accessibility, requiring significant investment. A high priority should be given to the development of standardisation and of new techniques in automated testing, as explained in the Packaging and Testing Roadmap. Testing at all levels for PIC verification, at the wafer level, at the chip level and at the package level to establish performance, yield and reliability is needed. Test also requires significant investments in a wide range of equipment, some of it expensive. The creation of open access measurement facilities for that purpose will accelerate this process. The JePPIX support centres can play a role in providing or sharing facilities, once established.

**Design software**

The potential of a generic integration process is determined to a large extent by the quality and the scope of the available design and modelling tools and the associated design kits or PDKs, which contain specific information for a foundry process, including component libraries containing validated building blocks and components as well as sophisticated photonic circuits. Component libraries avoid the situation in which every designer has to reinvent the wheel, by developing their own lasers, modulators and detectors, for example, which is common practice in today’s device-specific process development culture.

Due to the nature of the photonics design eco-system being developed, designers can also create their own IP in the form of design modules for a library component or circuit which could be used in-house to shorten design cycles but can also be licensed to other platform users to generate income. In this way knowledge can be accumulated in an effective way, leading to ever more complex and powerful circuit designs.

Development of library modules for components and circuits requires significant investments, because testing, optimizing and accurate characterization of the component will require a number of fabrication runs. Especially for parameterized modules, which offer the user design freedom in the choice of the component parameters such as the wavelength of a laser or its spectral width, the repetition frequency of a pulse laser, or the channel wavelengths of an AWG.

Further extension of the platform capabilities through extension of the component and circuit libraries will require a significant research effort and should be part of R&D programs over a longer period of time. This includes the development of the fabrication technology, as well as the development of additional capabilities in the software tools such as in wafer and circuit verification, design rule checking (DRC), layout versus schematic validation (LVS) and a top-down or schematic driven layout work flow, all of which are areas of interest in the short to medium term.

**Foundries for PICs and packaging services**

The extremely low cost of many micro-electronic chips has become possible through huge investments in batch processing in highly standardized, high-performance integration processes that have proved capable of providing the same or better performance than device-specific processes, but at much lower
costs. This has been made possible because the large investments required are paid back by a much larger applications market.

For generic photonic foundry technologies the situation is similar. Large upfront investments are necessary to develop processes with the high performance required to serve a large applications market, and a continued high investment level will be required in the future to achieve a steady increase in performance and capabilities. Investments should also be made both in qualification and library development for the existing processes as well as in the development of new releases of the foundry processes with increased capabilities and performance.

The market enabled by photonic foundry technology will be orders of magnitude larger than the market for the technology itself. We have seen in Silicon VLSI that huge fabs can prosper, but this situation has taken many years to reach maturity. Investment in generic technology is a strategic issue not just for the companies involved but on a European scale. It is, therefore, in the public interest that public-private investments should drive the technology and its markets to a level where commercial investors can take over and rapid market expansion can occur.

A special point of attention is in packaging technology for PICs. In the PARADIGM project the first steps towards development of a standardized package have been taken through standardization of the optical and electrical ports on the chip and package standardisation using off the shelf parts. Development of generic packaging technologies and open-access packaging foundries should, therefore, have a high priority in future public-private R&D programs. This high priority was also emphasized in Photonics21 workshops in preparation for HORIZON 2020 calls for 2016/17.

European leadership

At present Europe has a lead in generic InP-based foundry technology. This is because of strategic investments made by Europe's key players in Photonic Integration through a close cooperation enabled by the JePPIX platform, and supported by large R&D programs like EuroPIC, PARADIGM and the Dutch MEMPHIS project. The JePPIX success is an excellent example of how the European Framework Program has brought Europe the lead through the joint efforts of its key players.

Recently the US government followed the European initiative announcing large investments (220M$ programme over 2015-2019) in photonic foundry approaches.15


10. Training and Education Roadmap

The interest in development of ASPICs in MPW foundry runs is seen to be rapidly increasing, the need for ASPIC designers is therefore increasing equally quickly. In 2013 we fabricated over 80 new designs in MPW runs, significantly more than predicted in our 2012 roadmap. In the very near future this number could rise to perhaps 200/yr. As a designer cannot do much more than 5-10 new designs per year this would require tens of designers for these MPW runs only which is a significant expansion on the present situation.

To accommodate the rapidly increasing number of designs, more designers need to be trained. JePPIX has been organizing annual two-week photonic IC design training courses since 2006. These courses are focused on providing trainee designers with a background in integrated photonics design and technology and practical fab aspects. They include hands-on sessions with various software tools. Starting in 2013 a new type of training has been provided for experienced designers aimed at high level photonic IC design using foundry specific PDKs.
These five-day intensive courses have been organized all over the world. Furthermore, JePPIX software partners offer dedicated training sessions to get familiar with the software tools, as well as on-demand practical sessions, and JePPIX organizes one-day short courses, webinars and workshops in cooperation with design houses.

A large number of students have followed the training courses so far, which means that an increasing number of people working in the field are aware of the application potential of ASPICs. However, few of them continue with a specialisation in photonic IC design and, therefore, the effort on enlarging the number of experienced designers has to be increased:

- create sufficient opportunities for skilled designers and students to find a job as ASPIC designer, which is mainly a matter of market growth,
- integrate photonic IC design courses in the curricula of technical universities and other technical colleges, (this will increase the market),
- Increase the training offer by JePPIX and JePPIX partners.

11. About JePPIX

JePPIX stands for the Joint European Platform for Photonic Integration of Components and Circuits. JePPIX has been extremely successful in bringing the European InP community together as a coherent force dedicated to building a generic foundry technology infrastructure. Coordination is of key importance for the success of the generic approach since it requires coordination of the work of many independent businesses spread across process development, chip fabrication, packaging, software development, design and training. The JePPIX platform is presently recognized as the coordinating body by all the key players in the InP-based foundry approach and it is, therefore, the instrument par excellence for coordinating future development.

Because of the high degree of complementarity between InP technology and low-loss dielectric waveguide technology for a range of applications, and the organizational similarity in handling MPW runs, JePPIX is now supporting both InP and TriPleX technology.

At present JePPIX is legally represented by TU Eindhoven, it will become an independent organisation in due course. JePPIX is managed by a management board, which includes a full-time coordinator. It reports to the JePPIX partner board, which consists of representatives of the partners that contribute to the technological infrastructure, and representatives of the user and the designer communities.

JePPIX runs the following activities:

**Organization of MPW runs** on the four foundry processes that are presently available in the platform. It includes supplying the design kits and other design information and handling legal aspects (NDAs and licenses).

**Education and training.** JePPIX organizes yearly trainings in photonic IC design and technology and it is presently expanding its training offer in cooperation with its software partners to offer webinars and workshops.

**Roadmap.** JePPIX publishes a roadmap for technology development, applications development, cost and market development, education and training, and R&D investments. The roadmap is updated every two years.

**User and member platform.** JePPIX is building a member group of companies, universities and research organisations to create the technology eco-system and the value chain to reduce entry barriers.
About JePPIX

barriers to ASPICs development. JePPIX provides members with information and support for participation in foundry runs and information on applications for ASPICs. At present the member group numbers more than 250 organisations. Figure 10 shows where they come from. A significant portion of the JePPIX membership is formed from industry, both SMEs and larger companies.

Outreach activities. JePPIX is actively extending its outreach to SMEs and large companies throughout Europe and worldwide. This activity includes the JePPIX mentoring program as well as scouting and promotions.

Regional support centres. JePPIX stimulates the creation and operation of regional support centres worldwide. The centres reach out to potential users, helping them to find their way on the path to use of ASPICs in their own applications. Support covers design, manufacturing and testing of photonic ICs.

JePPIX membership is free. For more information about JePPIX or for becoming a member see: www.jeppix.eu

16 JePPIX partners are the foundries Oclaro (UK), Fraunhofer HHI (DE), SMART Photonics (NL) and Lionix (NL), software partners PhoeniX Software (NL), Photon Design (UK) and Filarete (IT), Equipment Manufacturers ASML (NL), Oxford Plasma Technologies (UK) and Aixtron (DE), and R&D institutes III-V Lab (FR), Cambridge University (UK), Politecnico di Milano (IT), Warsaw University of Technology (PL) and the COBRA Research Institute of TU Eindhoven (NL). COBRA is coordinating JePPIX.

JePPIX Membership

Figure 10 JePPIX currently has more than 250 members.

Figure 11 More than 50% of the JePPIX members are from industry.

JEPPIX ROADMAP 2015